Patent claims

1. An electrical diagnostic circuit for the testing and/or the diagnostic analysis of an integrated circuit having the following features:

- a plurality of external inputs ($E_n$) for receiving digital values,
- a plurality of essentially similar, series-connected switching units having the following features:
  - each switching unit is connected to in each case one external input ($E_n$) for receiving a test signal of an integrated circuit (14),
  - each switching unit in each case has an internal input for an input signal from a switching unit arranged upstream or downstream,
  - the switching units are constructed to be controllable in such a manner that an input signal present at the internal input of a switching unit, in dependence on a control signal ($c_n$) of the switching unit,
    - are forwarded either unchanged to the internal input of the switching unit in each case arranged downstream or to the circuit output and/or are fed back to an internal input of a switching unit arranged upstream,
    - or are combined with the test signal in each case present at the external input ($E_n$) and the combination value determined from this combination is forwarded to the internal input of the switching unit in each case arranged downstream or to the circuit output and/or is fed back to the internal input of a switching unit arranged upstream,
- a circuit output (116) for outputting an output value.

2. The electrical diagnostic circuit as claimed in claim 1, characterized in that each switching unit has

one gate each, particularly an exclusive OR gate ($XOR_n$), one multiplexer each ($MUX_n$) and one storage unit each ($D_n$).

3. The electrical diagnostic circuit as claimed in claim 2, characterized in that each external input ($E_n$) leads to one input each of the exclusive OR gate ($XOR_n$), each internal input leading to one external input each of the multiplexer arranged downstream ($MUX_n$) and, in parallel, to one second input each of the associated exclusive OR gate ($XOR_n$), each output of the exclusive OR gate ($XOR_n$) leading to one second input each of the multiplexer ($MUX_n$) and each output of the multiplexer ($MUX_n$) leading to one input each of the storage element ($D_n$), the output of which represents the output of the switching unit.

4. The electrical diagnostic circuit as claimed in claim 2 or 3, characterized in that the internal input of at least one switching unit, in dependence on the control signal ($c_n$) of the switching unit, is connected to the first input of the multiplexer ($MUX_n$) or to the second input of the exclusive OR gate ($XOR_n$).

5. The electrical diagnostic circuit as claimed in one of claims 1 to 4, characterized in that the electrical diagnostic circuit (10 - 13, 15, 16) has a controllable feedback unit (115, 214, 314), connected to the circuit output (116), which is constructed in such a manner that the output value is fed back to at least one internal input of a switching unit.

6. The electrical diagnostic circuit as claimed in claim 5, characterized in that the feedback unit (115, 214, 314) is present as a controllable gate (115, 214, 314), particularly as a controllable AND gate (115, 214, 314) and has a control signal input (123, 223, 313), the controllable gate (115, 214, 314) being constructed in such a manner that the output value is

be fed back to at least one internal input of a switching unit if a predetermined value is present at the control signal input (123, 223, 313).

7. The electrical diagnostic circuit as claimed in claim 5 or 6, characterized in that the switching units of the electrical diagnostic circuit (10 - 13, 15, 16) in each case have at least two, particularly series-connected storage units ($D_1$, $D'_1$; ...; $D_n$, $D'_n$), the output of the last storage unit ($D'_1$, ..., $D'_n$) in each case of each switching unit forming the output of the relevant switching unit.

8. The electrical diagnostic circuit as claimed in one of claims 5 to 7, characterized in that at least one further storage unit ($D_1$, ..., $D_n$), not belonging to a switching unit, is provided which is connected to the output of a switching unit of the electrical diagnostic circuit (10 - 13, 15, 16).

9. The electrical diagnostic circuit as claimed in one of claims 5 to 8, characterized in that the feedback unit (214, 314) has an OR gate ($XOR'_1$, 315), particularly an exclusive OR gate ($XOR'_1$, 315), one input of the controllable gate (214, 314) being connected to the output of the OR gate ($XOR'_1$, 315) and the inputs of the OR gate ($XOR'_1$, 315) being formed by at least two feedback lines (220 - 222; 324 - 325; 620 - 622) which in each case branch off after at least one switching unit and/or after in each case one storage unit ($D_1$, $D'_1$; ...; $D_n$, $D'_n$; $D'_{n+1}$; ...; $D'_r$).

10. The electrical diagnostic circuit as claimed in one of claims 5 to 9, characterized in that the feedback unit (115) has a further controllable gate (125), particularly a controllable AND gate (125), a controllable OR gate, a controllable NAND gate or a controllable NOR gate, the inputs of the further controllable gate (125) being formed by a further

control signal input (124) and by the output of the last switching unit, and the output of the further controllable gate (125) forming the circuit output (116).

11. The electrical diagnostic circuit as claimed in one of claims 5 to 10, characterized in that at least one further gate ($XOR'_3$), particularly an exclusive OR gate ($XOR'_3$) is provided which is in each case located between switching units arranged in series, the output value present at the circuit output (116) being conducted to an input of this further gate ($XOR'_3$).

12. The electrical diagnostic circuit as claimed in claim 1, characterized in that the first switching unit has an AND gate (44) and a storage unit ($D_1$) and in that all further switching units have one gate each ($XOR_2$ - $XOR_n$), particularly an exclusive OR gate ($XOR_2$ - $XOR_n$), one multiplexer each ($MUX_2$ - $MUX_n$) and one storage unit each ($D_2$ - $D_n$).

13. The electrical diagnostic circuit as claimed in claim 12, characterized in that the first external input ($E_1$) leads to the first input of the AND gate (44) and a control line (416) leads to the second input of the AND gate (44), the output of the AND gate (44) leading to the storage unit ($D_1$), the output of which represents the output of the first switching unit, and in that each further external input ($E_2$ - $E_n$) in each case leads to one input of the in each case associated exclusive OR gate ($XOR_2$ - $XOR_n$), each internal input of the switching units in each case leading to a first input of the downstream multiplexer ($MUX_2$ - $MUX_n$) and, in parallel, to a second input of the respective exclusive OR gate ($XOR_2$ - $XOR_n$), each output of an exclusive OR gate ($XOR_2$ - $XOR_n$) in each case leading to a second input of the downstream multiplexer ($MUX_2$ - $MUX_n$) and each output of the multiplexer ($MUX_2$ - $MUX_n$) in each case leading to an input of the

downstream storage element ($D_2$ - $D_n$), the output of which represents the output of the switching unit.

14. The electrical diagnostic circuit as claimed in claim 13, characterized in that for all switching units except the first switching unit, the internal input is connected to the first input of the multiplexer ($MUX_2$ - $MUX_n$) and to the second input of the exclusive OR gate ($XOR_2$ - $XOR_n$).

15. The electrical diagnostic circuit as claimed in one of claims 12 to 14, characterized in that the output (116) of the last switching unit is connected to a shift register with linear feedback.

16. The electrical diagnostic circuit as claimed in claim 15, characterized in that the shift register with linear feedback has an exclusive OR gate (415), a number of series-connected storage elements ($D'_1$, ..., $D'_m$) and at least one feedback line (427, 428), which branches off after a storage element ($D'_1$, ..., $D'_m$) and which leads/lead to in each case one input of the exclusive OR gate (415), the first storage element ($D'_1$) being connected to the output of the exclusive OR gate (415).

17. The electrical diagnostic circuit as claimed in one of claims 1 to 16, characterized in that a selection circuit, which is intended for controlling the electrical diagnostic circuit (10 - 13, 15, 16), is provided at the inputs ($E_n$) of the electrical diagnostic circuit (10 - 13, 15, 16).

18. The electrical diagnostic circuit as claimed in one of claims 1 to 17, which is integrated monolithically on the integrated circuit (14) to be tested and/or to be diagnosed.

19. A probe card for testing integrated circuits, the

probe card having an electrical diagnostic circuit as claimed in one of claims 1 to 18.

20. A load board for receiving a probe card for testing integrated circuits and/or with one or more test sockets for testing integrated circuits and/or for connecting a handler to a tester of integrated circuits, the load board having an electrical diagnostic circuit as claimed in one of claims 1 to 18.

21. A tester with measuring sensors, particularly for currents and voltages and with instruments for generating digital signals or datastreams, the tester having an electrical diagnostic circuit as claimed in one of claims 1 to 18.

22. A method for testing and/or for the diagnostic analysis of an integrated circuit, comprising the following steps:

a) providing an electrical diagnostic circuit (10 - 13, 15, 16) which has n external inputs ($E_n$) for receiving test data of n parallel datastreams of an integrated circuit (14) to be tested and/or to be diagnosed and which is capable of generating signatures from the received test data (u, t, s, r), the test data (u, t, s, r) present at the n external inputs ($E_n$) selectively being included or not included in the generation of the signatures,

b) connecting the electrical diagnostic circuit (10 - 13, 15, 16) to the integrated circuit (14) to be tested and/or to be diagnosed, in such a manner that the n inputs ($E_n$) of the electrical diagnostic circuit (10 - 13, 15, 16) are present at the n outputs ($A_n$) of the integrated circuit (14),

c) controlling the switching units of the electrical diagnostic circuit (10 - 13, 15, 16) in such a manner that the test data (u, t, s, r) in each case present at the external inputs ($E_n$) are

included in the generation of the signatures,

d) detecting and processing the test data (u, t, s, r) of the integrated circuit (14) to be tested and/or to be diagnosed to form at least one signature in one or in more successive test runs through the electrical diagnostic circuit (10 - 13, 15, 16),

e) checking the signature for correctness by means of the test by comparing the signatures determined in the test with the correct signature stored in the tester or determined by the tester,

f) if at least one errored signature has been determined in step e), carrying out the following steps:

g) performing k successive test runs, wherein in each case only those data, present at the input $E_i$, of the n datastreams in the jth run are included in the compacting in the electrical diagnostic circuit (10 - 13, 15, 16) if the binary coefficient $a_{i,j}$ of the equations for determining the control points of a linear separable error-correcting code with n information points $u_1, \ldots, u_n$ and with k control points $v_1, \ldots, v_k$ is equal to one, the k control points $v_1, \ldots, v_k$ being determined by the k binary equations

$$v_1 = a_{1,1}\ u_1 \oplus \ldots \oplus a_{1,n}u_n$$

$$\cdot$$

$$\cdot$$

$$\cdot$$

$$v_1 = a_{k,1}u_1 \oplus \ldots \oplus a_{k,n}u_n$$

from the n information points.

h) Determining the errored elements in the n datastreams, particularly the errored scan cells of the diagnosed integrated circuit (14) from the deviations of the observed output signatures output by the electrical diagnostic circuit (10 - 13, 15, 16) at its output (116, 326) in the

k test runs

$[y_1^b, y_2^b, y_3^b, \ldots]$

from the corresponding correct output signatures

$[y_1^k, y_2^k, y_3^k, \ldots]$.

23. The method as claimed in claim 22, characterized in that the datastreams are data which are shifted out of the scan paths ($SC_n$) of an integrated circuit.

24. The method as claimed in claim 22 or 23, characterized in that the electrical diagnostic circuit (10 - 13, 15, 16) provided in step a) is an electrical diagnostic circuit (10 - 13, 15, 16) as claimed in one of claims 1 to 18.

25. The method as claimed in one of claims 22 to 24, characterized in that the electrical diagnostic circuit (10 - 13, 15, 16) provided in step a) is constructed on a probe card as claimed in claim 19, on a load board as claimed in claim 20 or on a tester as claimed in claim 21.

26. The method as claimed in one of claims 22 to 25, characterized in that in step c), the switching units are activated by means of a control signal ($c_n$) in such a manner that the input signals present at the internal inputs of the switching units are combined with the test data (u, t, s, r) in each case present at the external inputs ($E_n$) and that the combination values in each case determined from these combinations are forwarded to the internal inputs of the switching units in each case arranged downstream.

27. The method as claimed in one of claims 22 to 26, characterized in that in method step d), all control signals $c_{i,j}$, $1 \leq i \leq k$, $1 \leq j \leq n$ of the multiplexers

($MUX_1$, ..., $MUX_n$) are selected to be one.

28. The method as claimed in one of claims 22 to 27, characterized in that, if the electrical diagnostic circuit (10 - 13, 15, 16) has a feedback unit (115; 125; 214; 314), it is activated before step c) in such a manner that it does not feed back.

29. The method as claimed in one of claims 22 to 27, characterized in that, if the electrical diagnostic circuit (10 - 13, 15, 16) has a feedback unit (115; 125; 214; 314), it is activated before step c) in such a manner that it does not feed back.

30. The method as claimed in one of claims 22 to 29, characterized in that the method step g) is carried out as follows:
carrying out k successive test runs, wherein a control point ($v_k$) is determined with each run in accordance with the following rule from the information points ($u_n$) until all control points ($v_k$) have been determined,

$$v_1 = a_{1,1}u_1 \oplus \ldots \oplus a_{1,n}u_n$$

$$\vdots$$

$$v_k = a_{k,1}u_1 \oplus \ldots \oplus a_{k,n}u_n$$

wherein the coefficients $a_{i,j}$ with $1 \leq i \leq k$, $1 \leq j \leq n$ assume the values zero or one, the switching units of the electrical diagnostic circuit (10 - 13, 15, 16) being controlled in such a manner that the test data (u, t, s, r) present at the jth external input ($E_j$) in the ith run are only subjected to a combination in the switching units if the control signal $c_{i,j}$, with $1 \leq i \leq k$, $1 \leq j \leq n$, assumes the value one, whereby the control signal $c_{i,j}$ assumes the value zero if the associated coefficient $a_{i,j}$ assumes the value zero or if an indeterminate value in the datastream is to be

blanked out.

31. The method as claimed in one of claims 22 to 29, characterized in that the value of the control signal present at the first input (124) of the AND gate (125) assumes the value zero if an indeterminate value is present at the output of the upstream storage element $D_n$, and thus at its second input.

32. The method as claimed in one of claims 22 to 31, characterized in that method step g) is carried out as follows: carrying out k successive test runs by the switching units of the electrical diagnostic circuit (10 - 13, 15, 16) being controlled in accordance with the binary coefficients $a_{i,j}$ of the equations for determining the control points $v_1, \ldots, v_k$ of a linear separable error-correcting code with n information points $u_1, \ldots, u_n$ and with k control points $v_1, \ldots, v_k$, in such a manner that the test data (u, t, s, r) present at the jth external input ($E_j$) in the ith run are only subjected to a combination in the switching units of the electrical diagnostic circuit (10 - 13, 15, 16) when the binary control signal $c_{i,j}$, with $1 \le i \le k$, $1 \le j \le n$, assumes the value one, whereby the control signal $c_{i,j}$ assumes the value zero when the associated coefficient $a_{i,j}$ in the linear equations for determining the k control points of the error-detecting code assumes the value zero or when an indeterminate value in the datastream is to be blanked out, the k control points $v_1, \ldots, v_k$ being determined from the k binary equations

$$v_1 = a_{1,1}u_1 \oplus \ldots \oplus a_{1,n}u_n$$

$$\vdots$$

$$v_k = a_{k,1}u_1 \oplus \ldots \oplus a_{k,n}u_n$$

from the n information points.

33. The method as claimed in one of claims 22 to 32, characterized in that the multiplexers ($MUX_n$) of the switching units are controlled by the control signals ($c_n$).

34. The method as claimed in one of claims 22 to 33, characterized in that a selection circuit which controls the input into the electrical diagnostic circuit (10 - 13, 15, 16) is provided between the outputs ($A_n$) of the integrated circuit (14) and the inputs ($E_n$) of the electrical diagnostic circuit (10 - 13, 15, 16).

35. Using the method as claimed in one of claims 22 to 34 for testing and/or for the diagnostic analysis of printed board assemblies or of circuit boards.

36. A computer program for carrying out a method for testing an integrated circuit, which is constructed in such a manner that the method steps c) to h) according to one of claims 22 to 34 can be executed.

37. The computer program as claimed in claim 36 which is contained on a storage medium, particularly in a computer memory or in a random access memory.

38. The computer program as claimed in claim 36 which is transmitted on an electrical carrier signal.

39. A data carrier comprising a computer program as claimed in claim 36.

40. A method in which a computer program as claimed in claim 36 is downloaded from an electronic data network such as, for example, from the Internet to a computer connected to the data network.